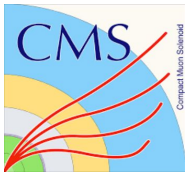
An ATCA Processor for Level-1 Trigger Primitive Generation and Readout of the CMS Barrel Muon Detectors

15.6.2022

HEP2022 - 39th Conference on Recent Developments in High Energy Physics and Cosmology, Thessaloniki, Greece



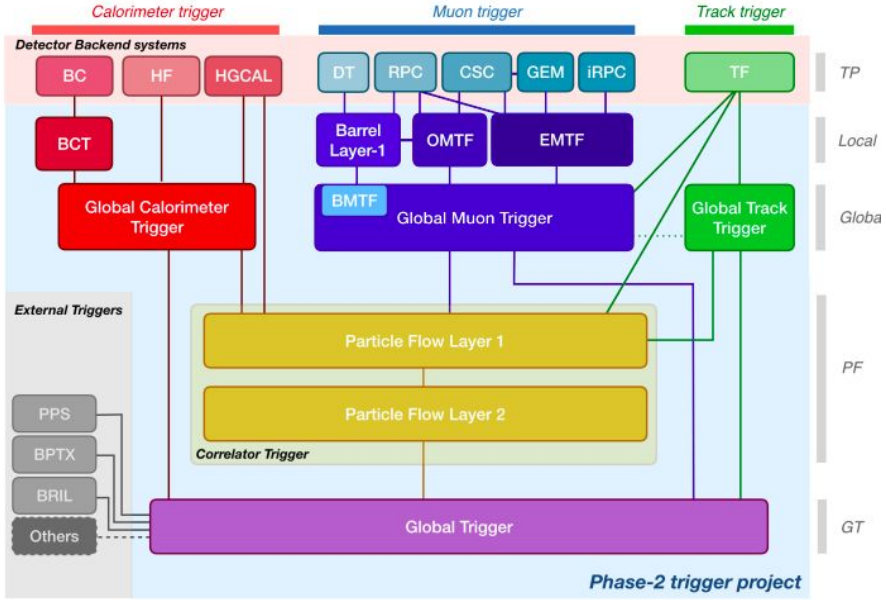
Ioannis Bestintzanos, BMTL1 team

CMS Phase 2 trigger - Drivers for new electronics

- The CMS trigger consists of various subsystems, each responsible for a specific task

- During the HL-LHC upgrade of the LHC, the luminosity is planned to increase by an order of magnitude
  - Current trigger can't handle these rates

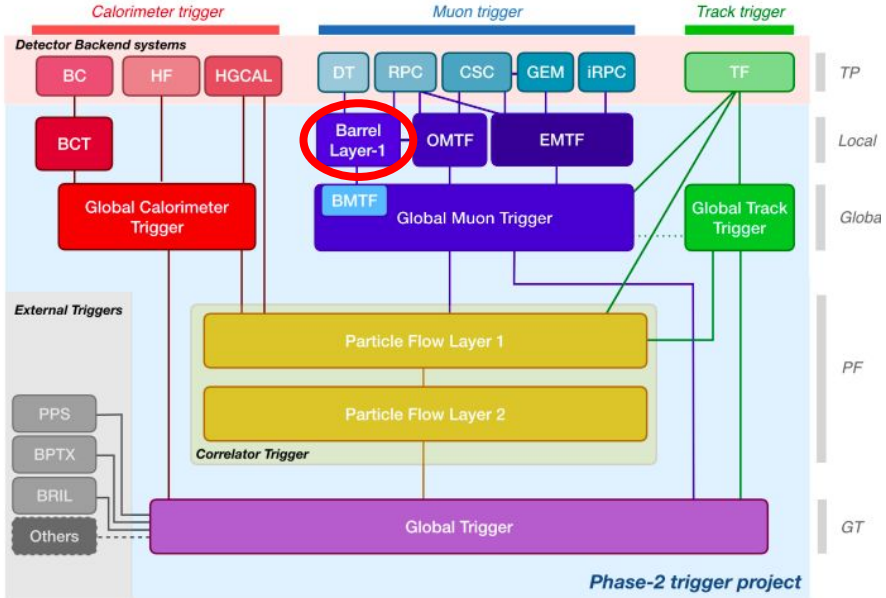
- This asks for upgraded electronics that can handle the increased data rates, but to also be able to accomodate more complicated algorithms, which will increase the physics-wise trigger efficiency



CMS Phase-2 L1 upgraded trigger scheme

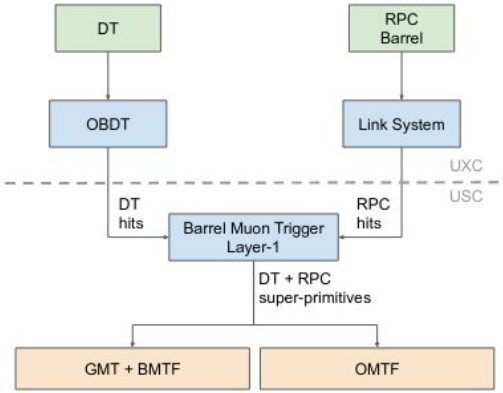
BMTL-1 in the trigger architecture

- Receives input directly from electronics on the detector
- Inputs from DTs and RPCs
  - 10 Gbps optical
- Outputs to the GMT and the scouting system
  - 25 Gbps optical
- Will host the analytical method algorithm, which takes advantage of the significantly improved time resolution of the on-detector electronics
- Asks for high processing power, as well as a large amount of optical connectivity
- ATCA architecture is the experiment standard



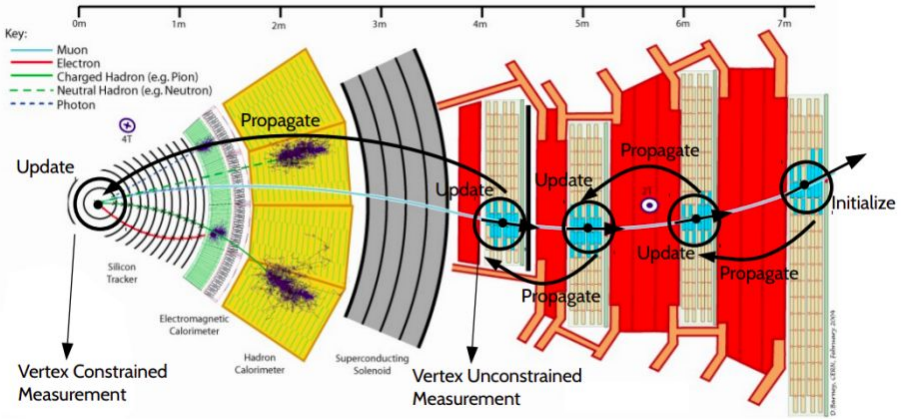
CMS Phase-2 L1 upgraded trigger scheme

BMTL-1 in the trigger architecture

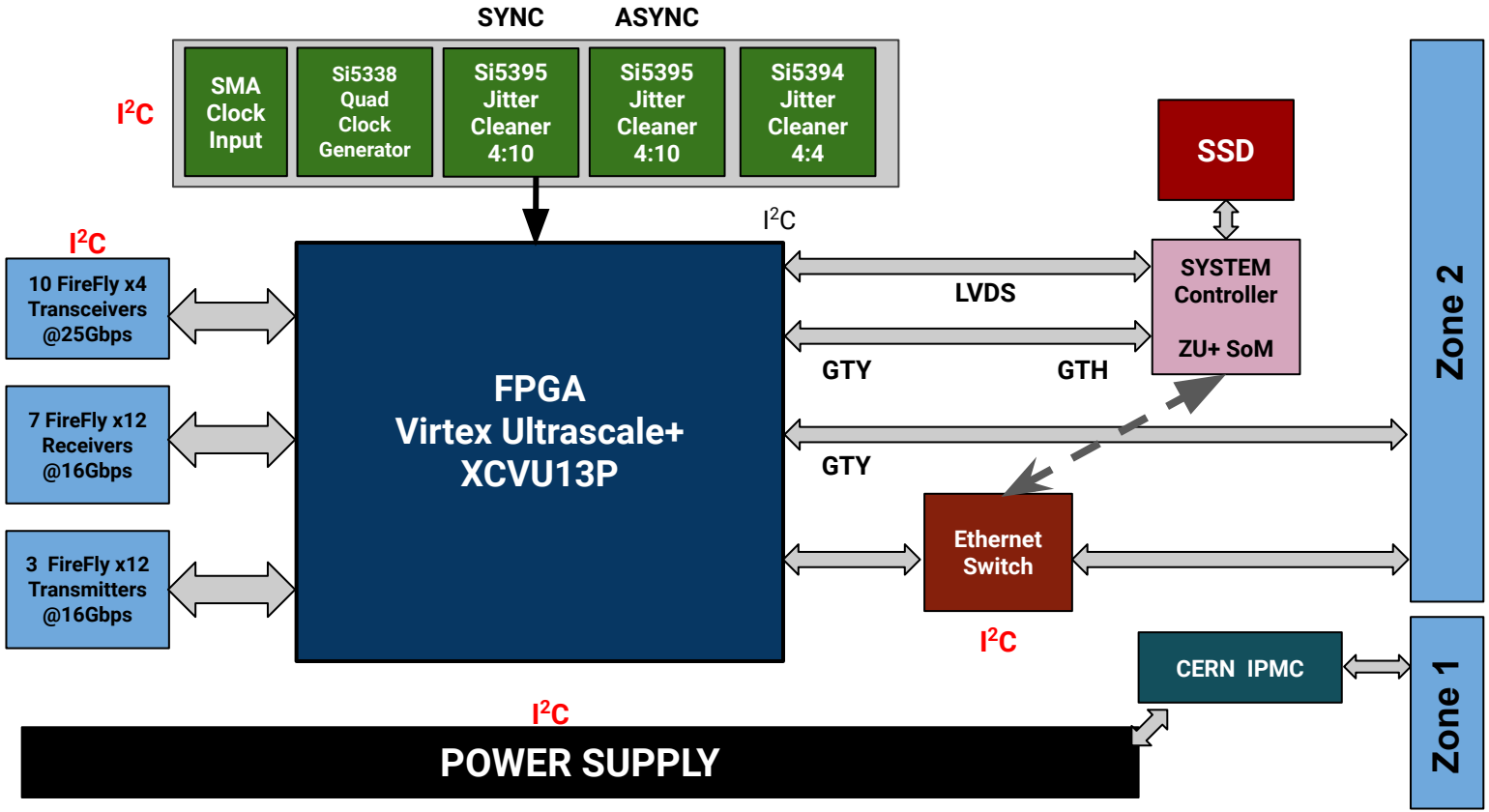


- Barrel Muon Trigger Layer-1 (BMTL-1) is the trigger subsystem responsible for reading data from the Drift Tubes (DTs) and the Resistive Plate Chambers (RPCs), directly from the detector. Information will be merged and combined into super-primitives, streamed to downstream systems

- BMTL-1 creates the track segments for the muon candidates, which are then forwarded downstream to the Global Muon Trigger (GMT), which joins the segments to create Muon tracks



Architecture of BMTL-1 ATCA board



FPGA used - XCVU13P

- **Xilinx XCVU13P FPGA**
  - *Ultrascale+ architecture*
  - *16 nm lithography*
  - *4 SLRs (Super Logic Regions)*
  - *1,728,000 LUTs*
  - *3,456,000 Flip Flops*
  - *12,288 DSP slices*
  - *128 GTY transceivers @ 28G*
  - *2577 ball BGA package*
  - *-1 speed grade*

- **Capability to use VU9P, VU11P**
  - Design is drop-in compatible with these two smaller FPGAs, with only compromise a slight drop in connectivity

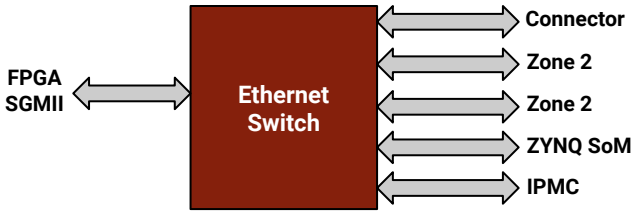
XCVU13P FPGA mounted on the BMTL-1 ATCA board

BMTL-1 ATCA board connectivity

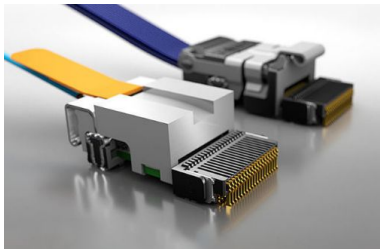
Optical connectivity

- **40 RX @ 25 Gbps** ⇨ *10 x BiDir FireFly Modules 25G*
- **40 TX @ 25 Gbps**
- **80 RX @ 16 Gbps** ⇨ *7 x Rx FireFly Modules 16G*
- **36 TX @ 16 Gbps** ⇨ *3 x Tx FireFly Modules 16G*

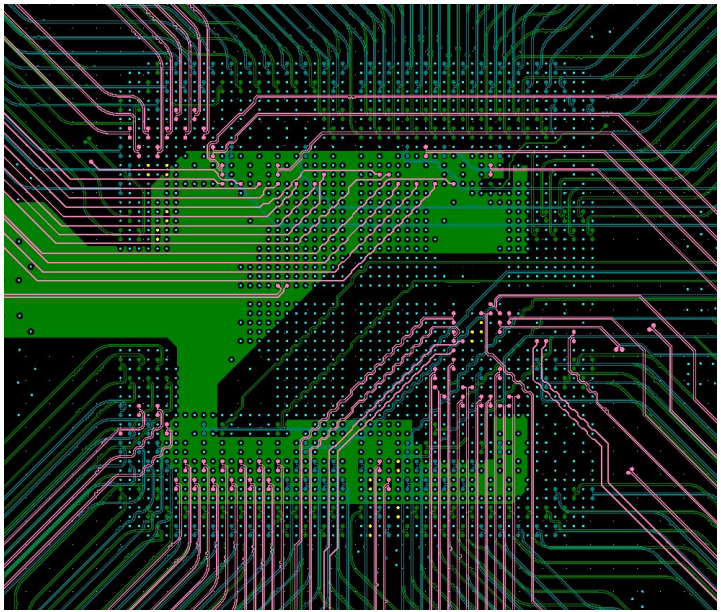
- **120** RX + **76** TX ~ **3.9** ***Tbps***



Onboard Ethernet switch circuitry provides access to many subsystems on board



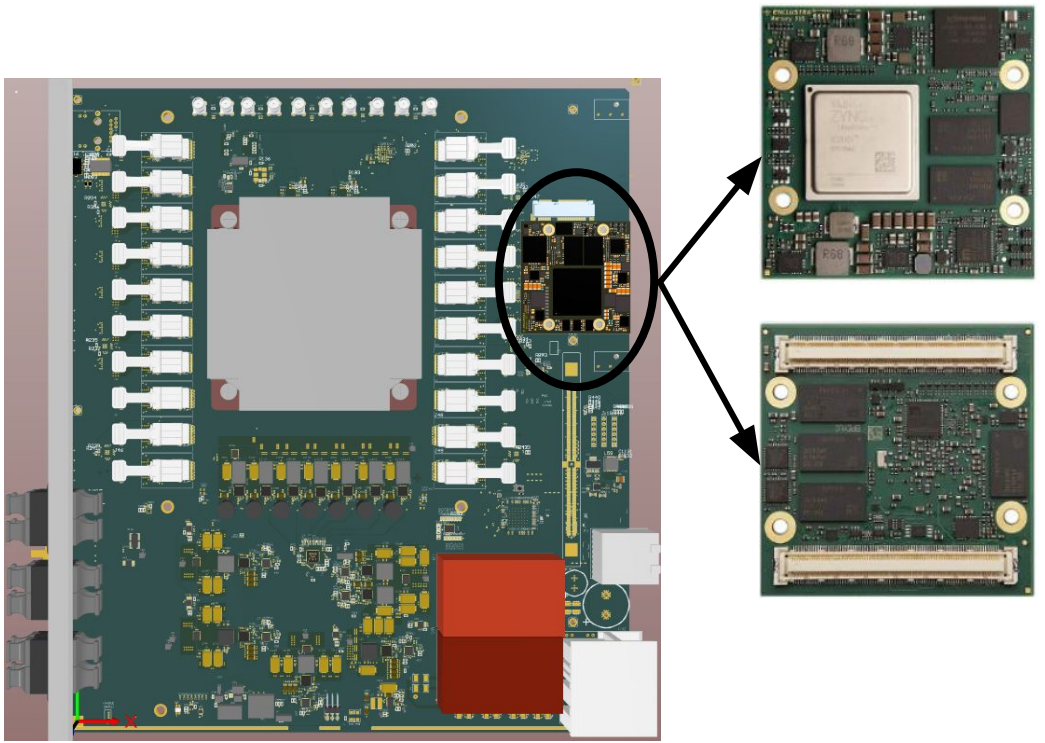
Samtec FireFly optical modules



Dense high-speed signal fanout under the FPGA

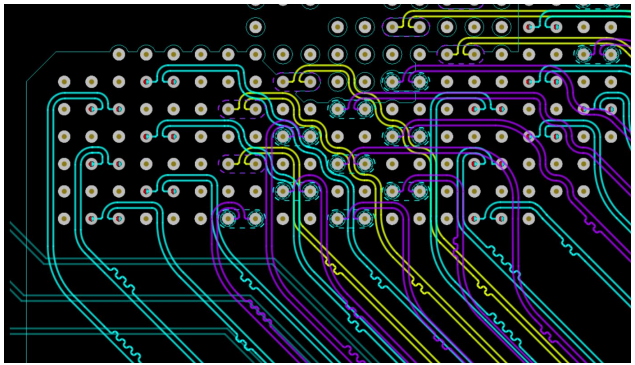
BMTL1 ATCA board system controller

- Enclustra Mercury XU5
  - *XCZU5EV-1FSVC784E SoC*
- Zynq Ultrascale+ architecture
- Quad core Arm Cortex A-53
  - *Capable of running Linux*
- Independent RAM on PS & PL
  - *2 GB (PS)*
  - *1 GB (PL)*
- Direct connections with the FPGA
  - 4 GTH MGTs @ 10G
  - 20 LVDS pairs
- SSD storage

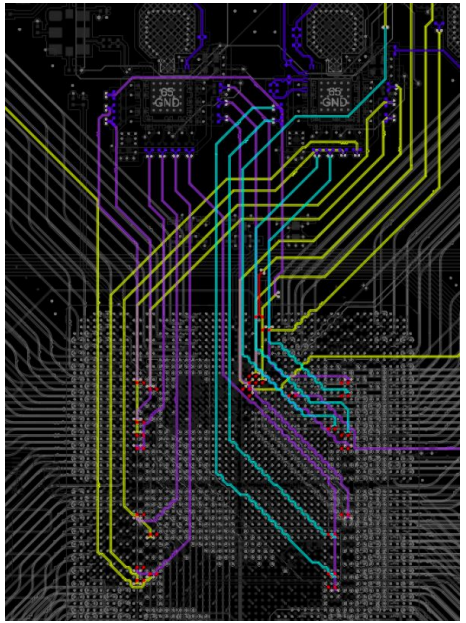


Design challenges

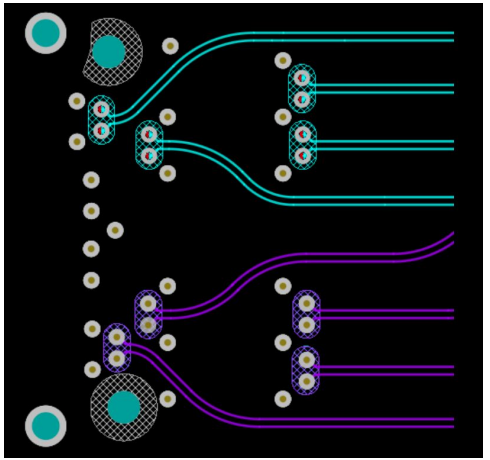
- Clocking
  - *Has to serve a large amount of links*
  - *Has to be very low jitter*
  - *Needs to be compatible with many operating scenarios*
- Signal integrity
  - *PCBs are very lossy at 25 Gbps*
  - *Very low loss dielectric material being used*
  - *Special design considerations for RF frequencies*
  - *Special technologies for PCB fabrication*
    - *Blind vias*
    - *Backdrilling*



High speed signal fanout under FPGA



Highlighted part of the clocking network

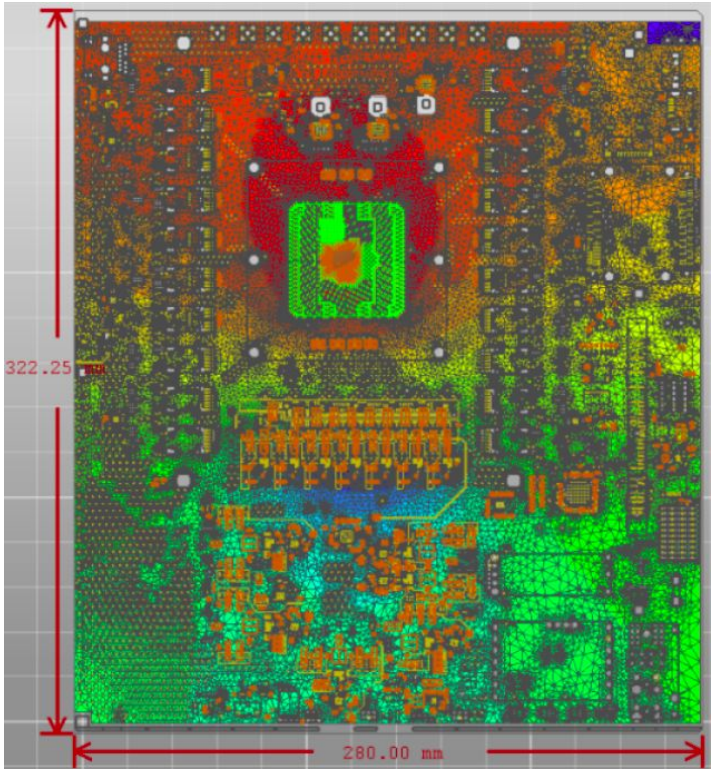


High speed signal routing detail. Avoidance of sharp edges is critical for signal integrity.

Design challenges

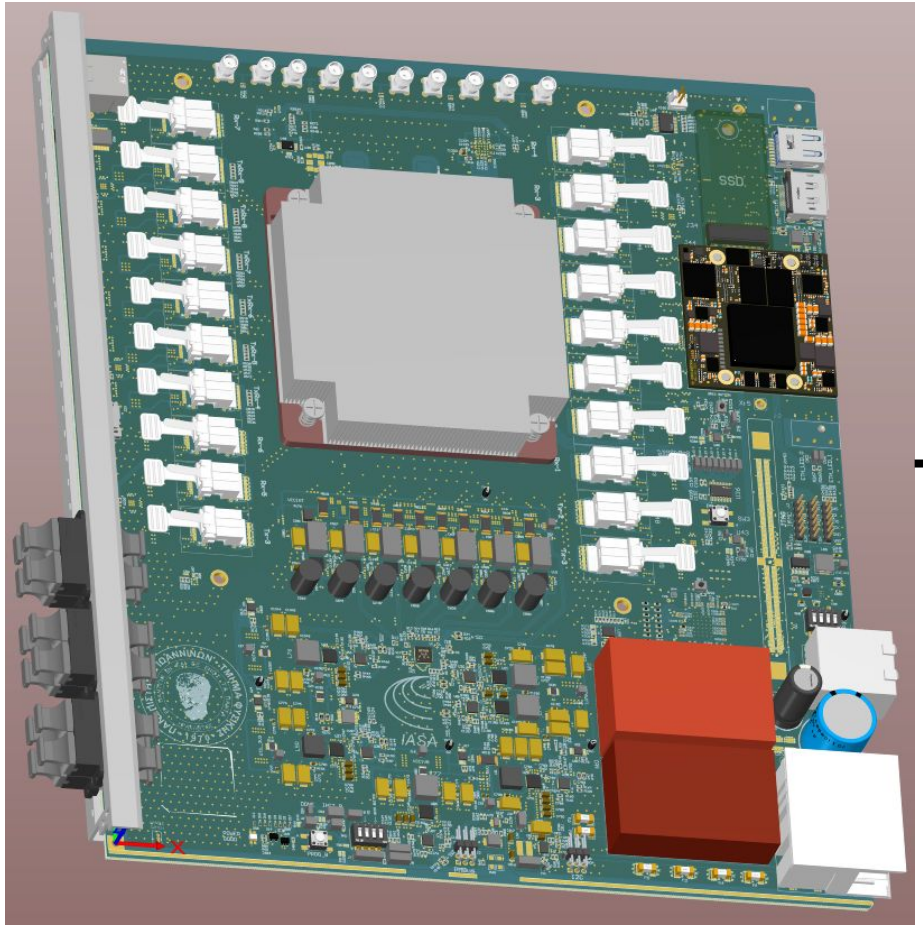
- Power delivery
  - *Core rail can consume in excess of 200A*
  - *Generation and delivery of such currents is not trivial*
- Thermal design
  - *The FPGA can dissipate more than 200W*
  - *Firefly optics reliability sensitive to high temperature*
  - *Extensive simulation of the card's thermal performance*
    - *Allowed for optimal component placement and aids optimal heat sink design*
  - *Custom heatsinks under design*
    - *Independent block heatsinks for the FPGA and the FireFlies*

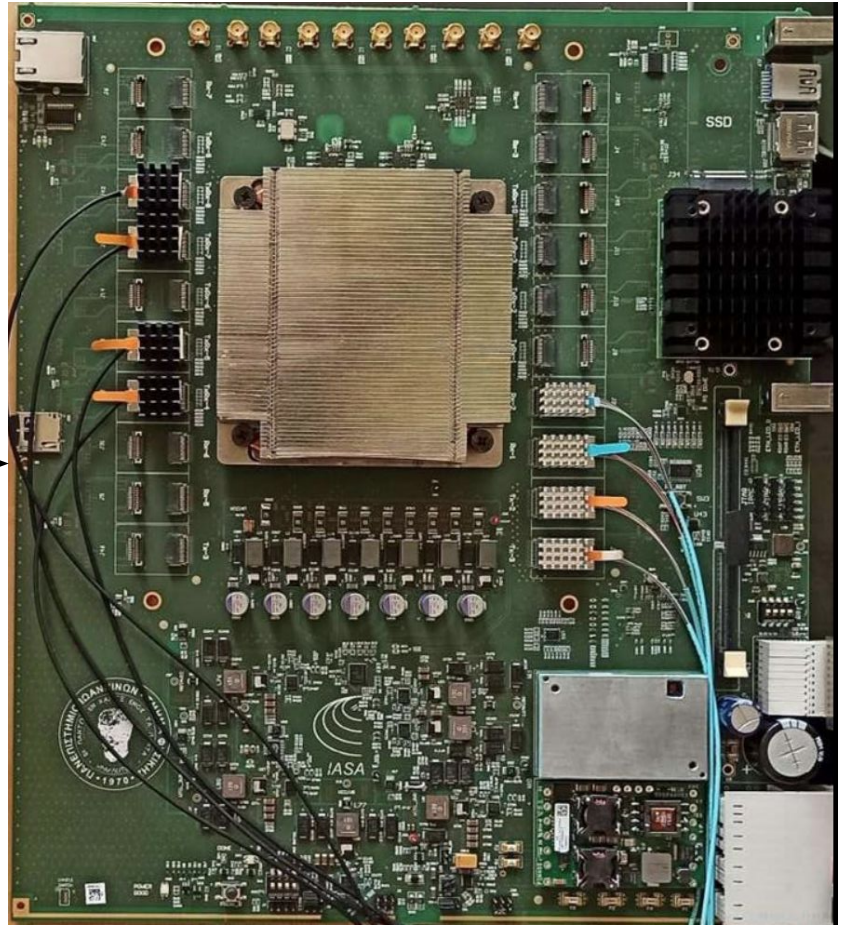
Core voltage power stage comprised of 7 phases



IR simulations proved very useful in optimizing current delivery

BMTL1 ATCA board

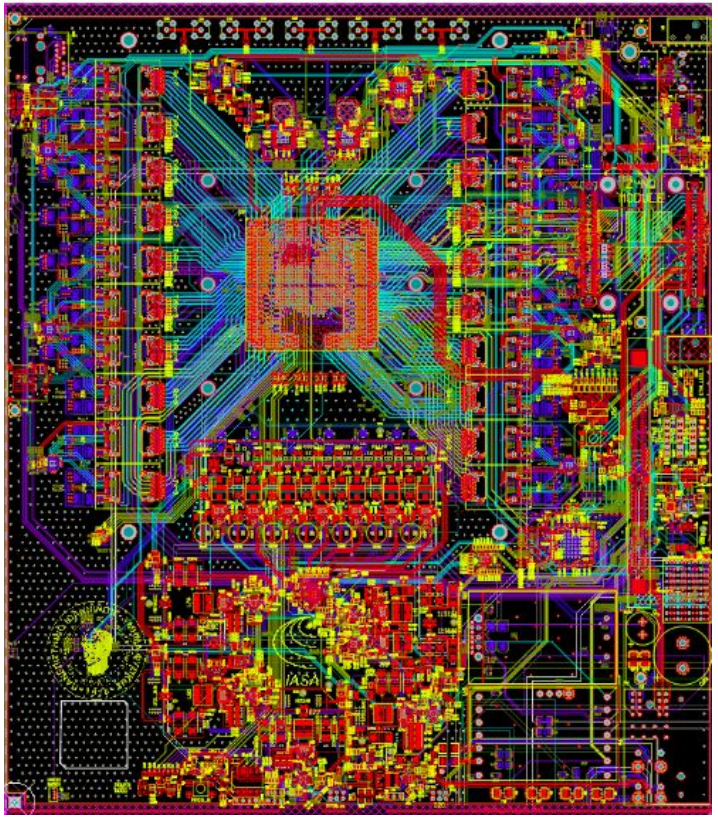




BMTL1 ATCA board assembly

- Original plan was to assemble 1 board without the FPGA
  - *To test functionality without risking FPGAs*
- Then proceed to assemble 2 boards with the FPGAs
  - *After the functionality had been verified*
- Assembler mistakenly assembled the FPGA on the first board
  - *Built another one without the FPGA*
    - Added more delay time

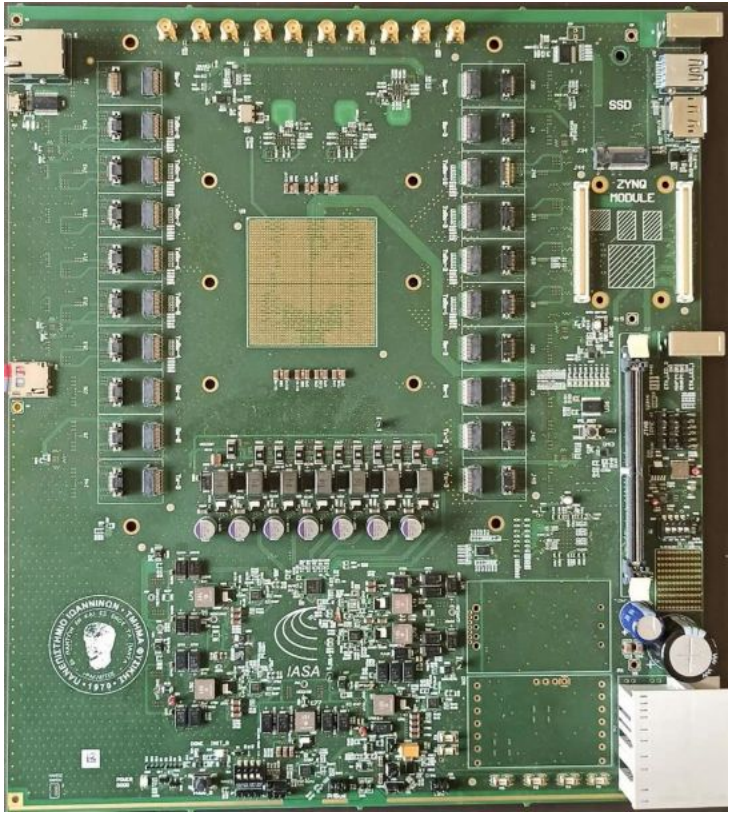
Two boards received beginning of May



First tests on the board without the FPGA

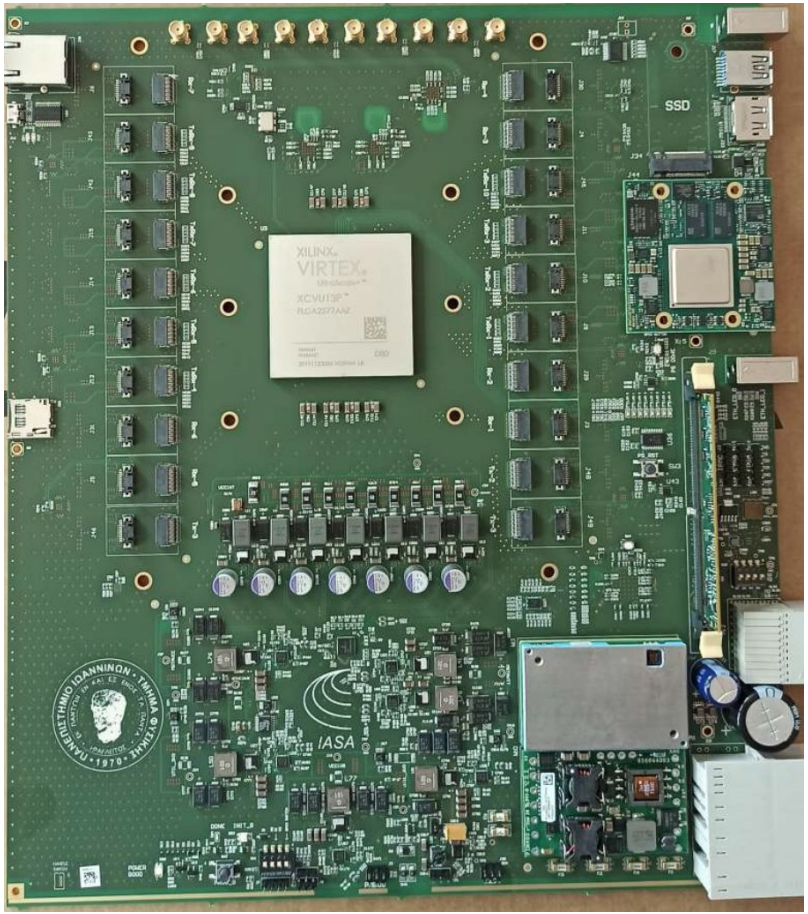
- This board proved very useful since it allowed verification and configuration of the power circuitry and the ZYNQ - Could not be done to the FPGA board
  - Stress-tested power supplies
    - *All power rails were stressed at 45+ Amps for a long time to observe the operation and ensure stability and thermals*
  - Tested the Zynq Enclustra module
    - Zynq appeared in Vivado, build Ubuntu image and boot from SD card, run Python scripts to configure clocks and Fireflies
  - Configured and verified Ethernet Switch
    - Internet from Front Panel RJ45 and Backplane - Zynq can access the Internet

- **This Board is still operating as a development platform - particularly useful for ZYNQ**



First tests with the FPGA board

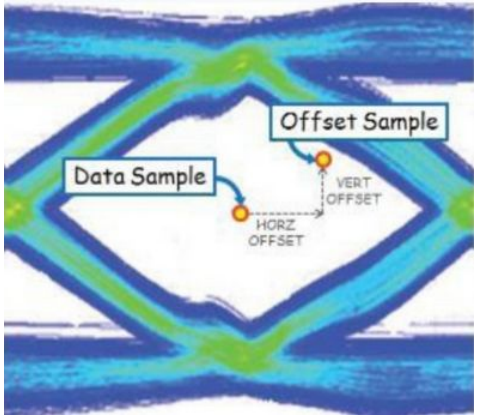
- After enough information were gained from the no-FPGA board, we started working on the one with the FPGA
- Power on went smoothly without issues
- XCVU13P appeared on Vivado
- First tests done with IBERT bit files
  - *Test clocks, link stability by counting errors, link quality with eyes*
- After taking the first eyes more MGTs were instantiated and scanned all possible 16G and 25G links

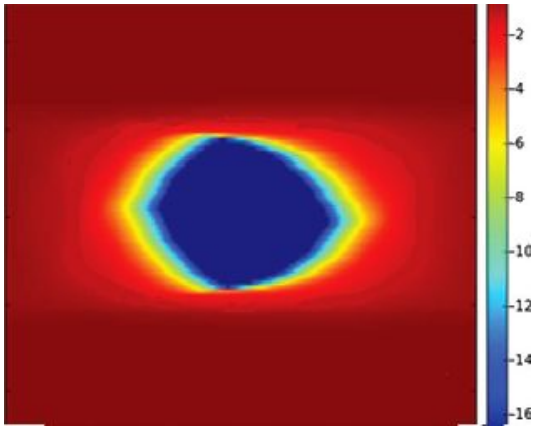


Signal integrity metrics

- **Eyescan**
  - Data sampler : samples in the middle of the eye
  - Offset sampler : samples anywhere in the eye
  - Difference between the data sampled by the two samplers, reveals the RX margin
  - Built-in functionality in many MGTs
  - Produces the eye diagram

- **Bit Error Rate (BER)**
  - Number of bit errors divided by the total number of transferred bits

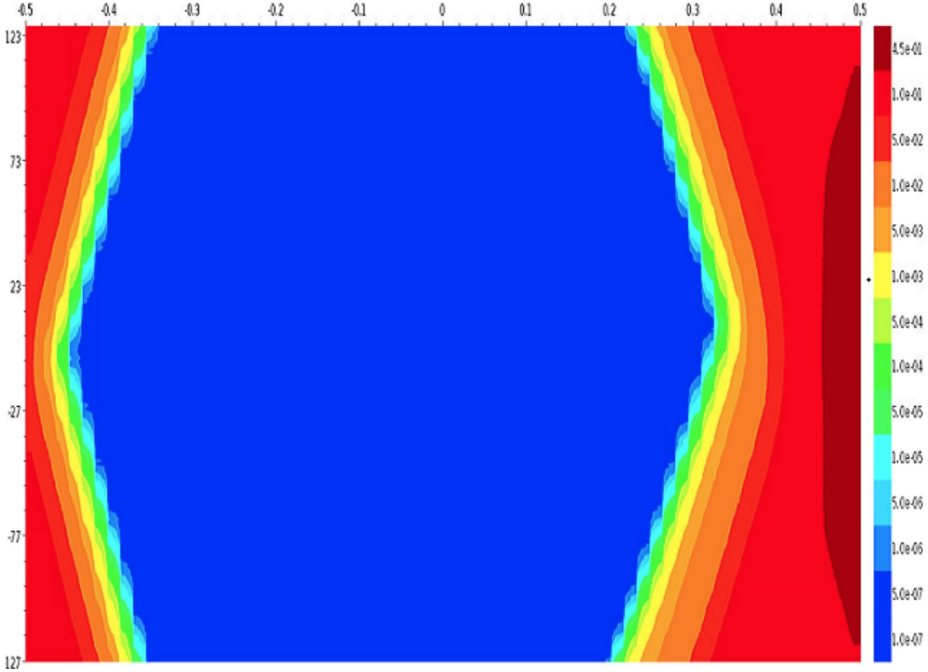




First 25G Eyescan

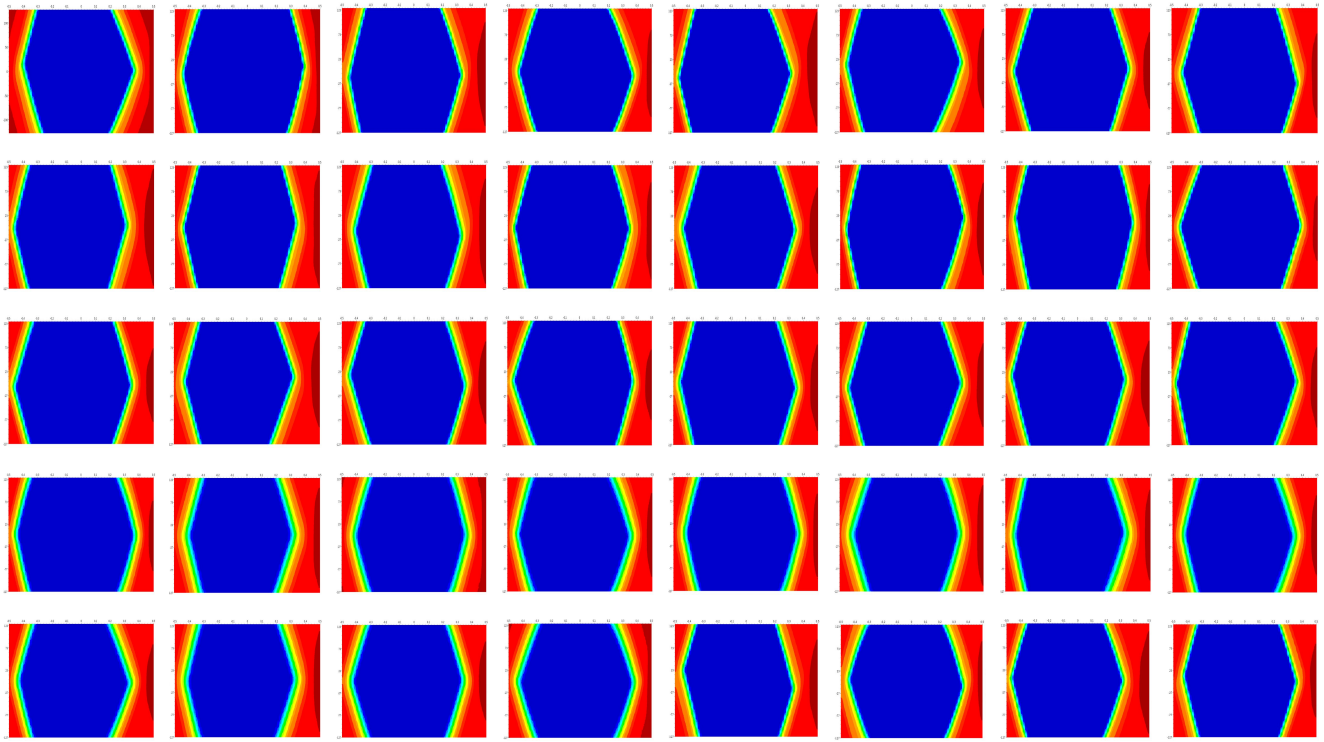
- **First eye taken**
  - *GTY @ 25 Gbps*
  - *External loopback w/ fiber*

- **This eye and all the rest shown, have been taken at *suboptimal* conditions, that is :**
  - **MGTAVTT operating using only 1 phase**
    - ***Critical for the performance***
  - **Power rails were still in debug mode**
    - ***Allowed their isolation, using voltage feedback behind the shunt resistors***
    - ***Caused voltage drop on the rails***
    - ***Now turned to operation mode, which already shows better results***



First eye-scan taken from a GTY transceiver on-board, using external loopback with 2m fiber

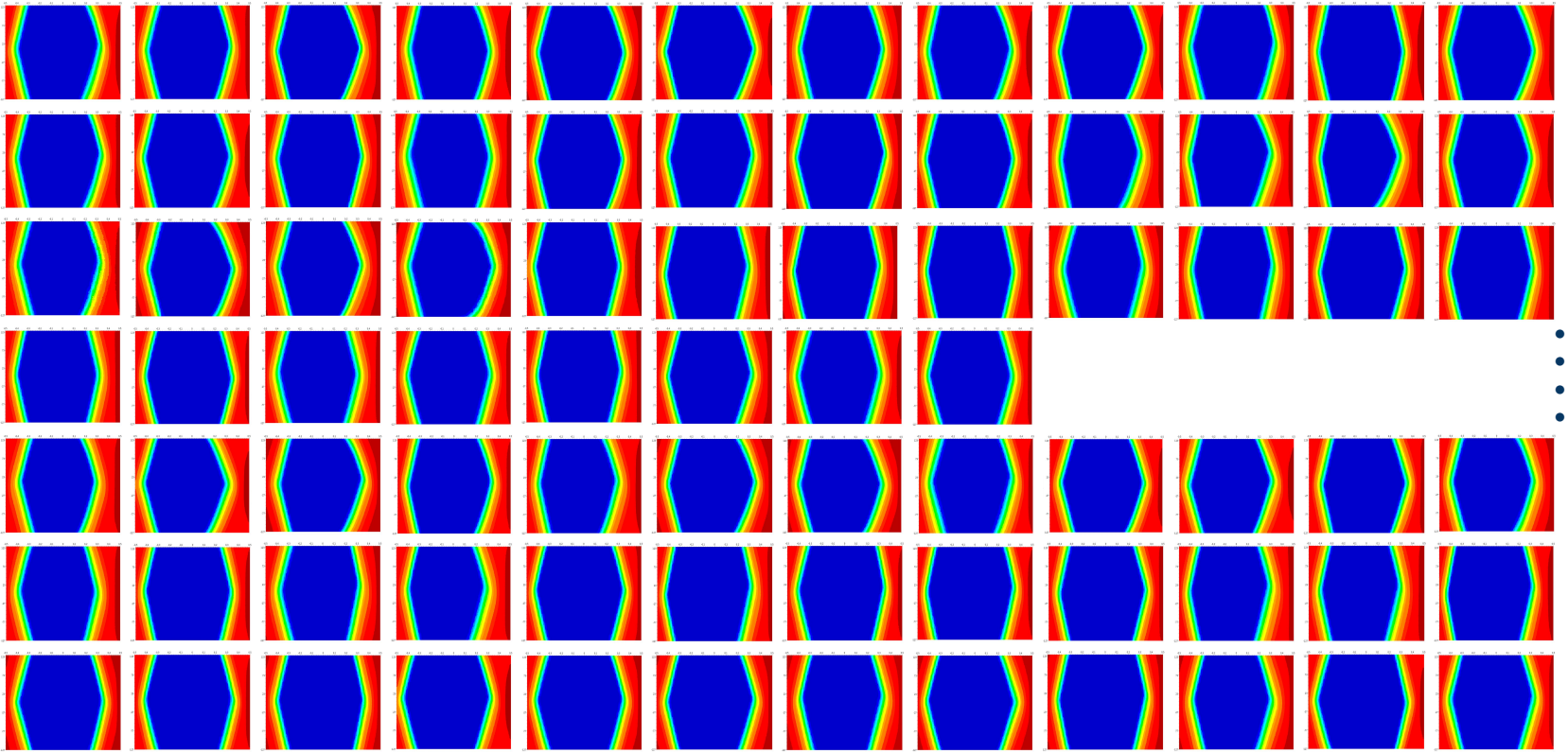
25G Eyescans



IBERT with all 40 25G MGTs instantiated and operating simultaneously

- **2 meter optic fiber**
- **25.6 Gb/s**
- **PRBS7**
- **Resolution 1**
- **Eyescan BER 1e-8**

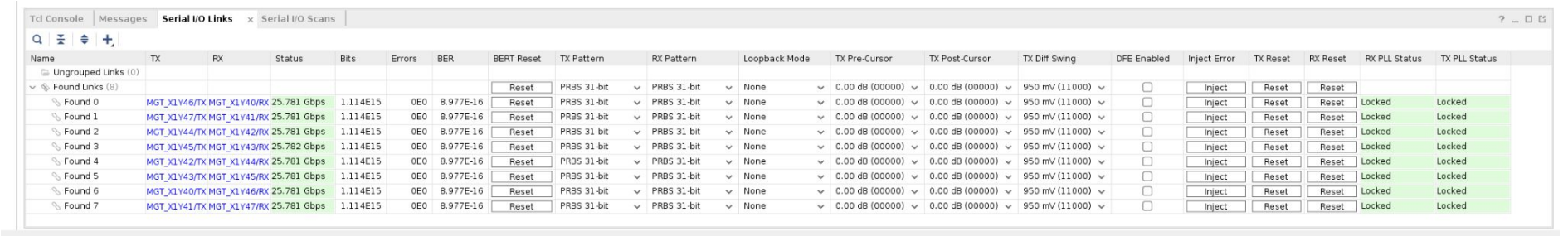
16G Eyescans



IBERT with all 80 16G MGTs instantiated and operating simultaneously

- **12 meter optic fiber**
- **16 Gb/s**
- **PRBS31**
- **Eyescan BER 1e-8**

25G Links Operation



Tcl Console | Messages | **Serial I/O Links** | Serial I/O Scans

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	Loopback Mode	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status
Ungrouped Links (0)																			
Found Links (8)							Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset		
Found 0	MGT_X1Y46/TX	MGT_X1Y40/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 1	MGT_X1Y47/TX	MGT_X1Y41/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 2	MGT_X1Y44/TX	MGT_X1Y42/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 3	MGT_X1Y45/TX	MGT_X1Y43/RX	25.782 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 4	MGT_X1Y42/TX	MGT_X1Y44/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 5	MGT_X1Y43/TX	MGT_X1Y45/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 6	MGT_X1Y40/TX	MGT_X1Y46/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked
Found 7	MGT_X1Y41/TX	MGT_X1Y47/RX	25.781 Gbps	1.114E15	0E0	8.977E-16	Reset	PRBS 31-bit	PRBS 31-bit	None	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)		Inject	Reset	Reset	Locked	Locked

- BER was tested down to ~9 x 10E-16 / link
  - **No errors appeared**
  - Will be tested for even less BER when more optical supplies arrive

Further Operational Tests

- Stress tested power supplies
  - *All rails stressed up to 45A with external load*
- VCCINT stressed up to 125A
  - *To be stressed more with adequate cooling*
  - *Power supply limit is 400+ A, so still a lot of headroom*
- Tested all clocks using oscilloscope and IBERT links
- Board inserted in crate and shows good mechanical fit
  - *Did not fit it all the way in*
  - *Should try again when we have a front panel*

✅ Tested all I2C devices

✅ Tested external clocks

✅ Tested all fireflies

✅ Tested Ethernet (switch circuitry)

Front Panel
Zone 2
ZYNQ

✅ Tested Zone 1 & 2

✅ Tested UART

✅ Tested SD

Further Developments

- ZYNQ - System Controller
  - Finalize functionality for access/control of the FPGA
  - Software for controlling on-board peripherals
- FPGA - Integrate EMP Framework
  - Provides control of the FPGA firmware over ZYNQ
  - Includes functionality such as CSP, GBT, LpGBT link protocols, TTC & TCDS, etc.
- Develop custom designed Heatsinks
  - One for the FPGA and two for the the Fireflies
  - Will occupy most area on the PCB
  - Optimized cooling efficiency - will allow to reach high power dissipation
- Manufacture Front Panel
- IPMC firmware development
- Production of one more fully populated board in the coming weeks

Conclusion

- An ATCA board meeting the specifications of the BMTL-1 was designed
- PCBs were produced
- Two boards were assembled
- The functionality of the design was tested and verified
- One more board to be produced soon
- Further developments are already on-going