The NSW High Voltage Infrastructure

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Outline

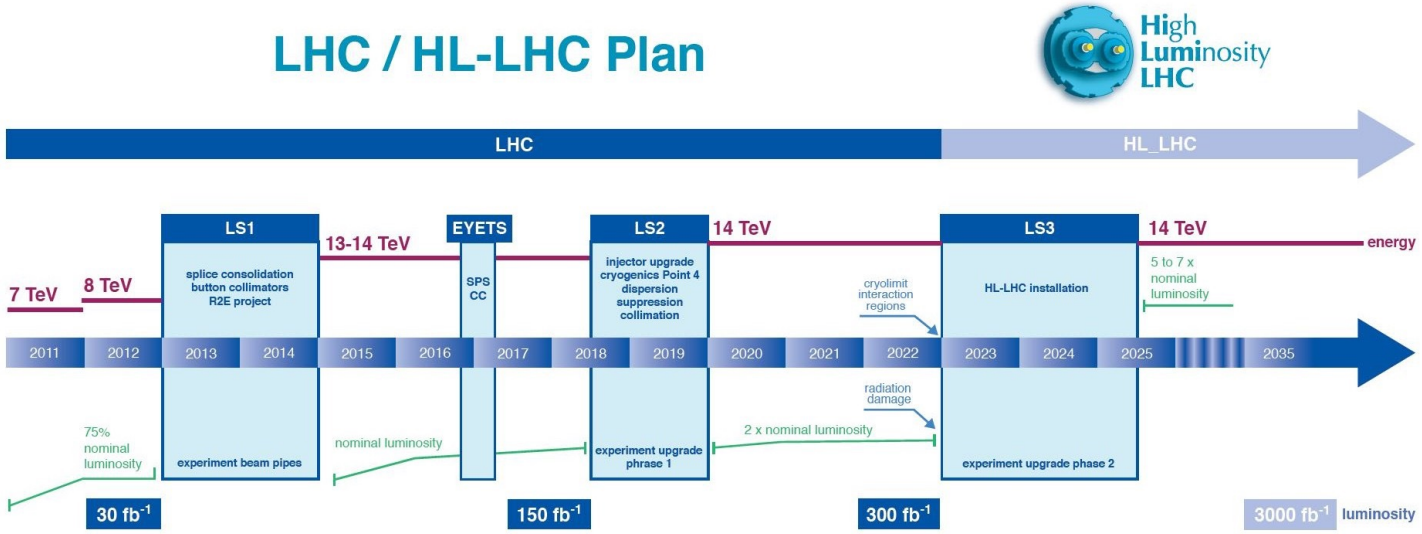
- ***The NSW High Voltage Infrastructure***

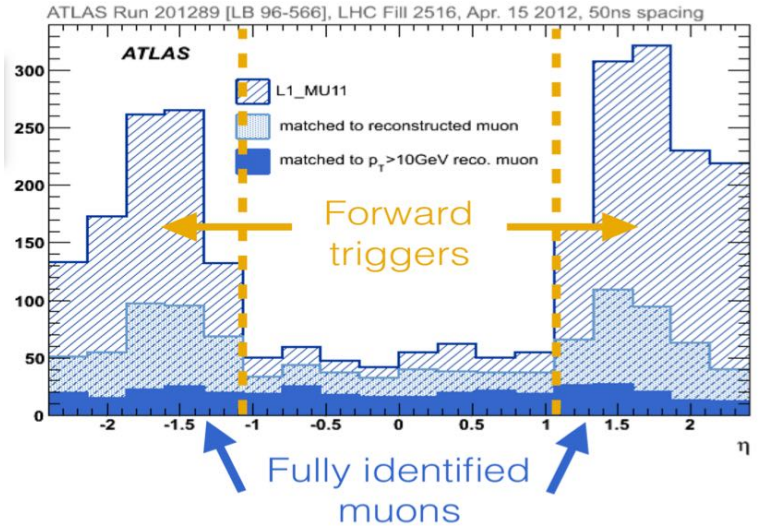
1. MMG/STG High Voltage Scheme
2. Hardware Installation
3. Validation of High Voltage Boards

- ***NSW HV DCS Integration***

1. NSW Caen Easy System
2. STG Caen Generators
3. NSW Reset Network

LHC Plan





The LHC upgrade aims to extend and to improve the physics discoveries by increasing the luminosity.

- Phase 1: 2018-2021, Luminosity up to 3 x 10^{34} $cm^{-2}s^{-1}$
- **Right now :**First beam splashes and collisions at 900 GeV after NSW commission
- Phase 2: 2024-2027, Luminosity up to 7.5 x 10^{34} $cm^{-2}s^{-1}$

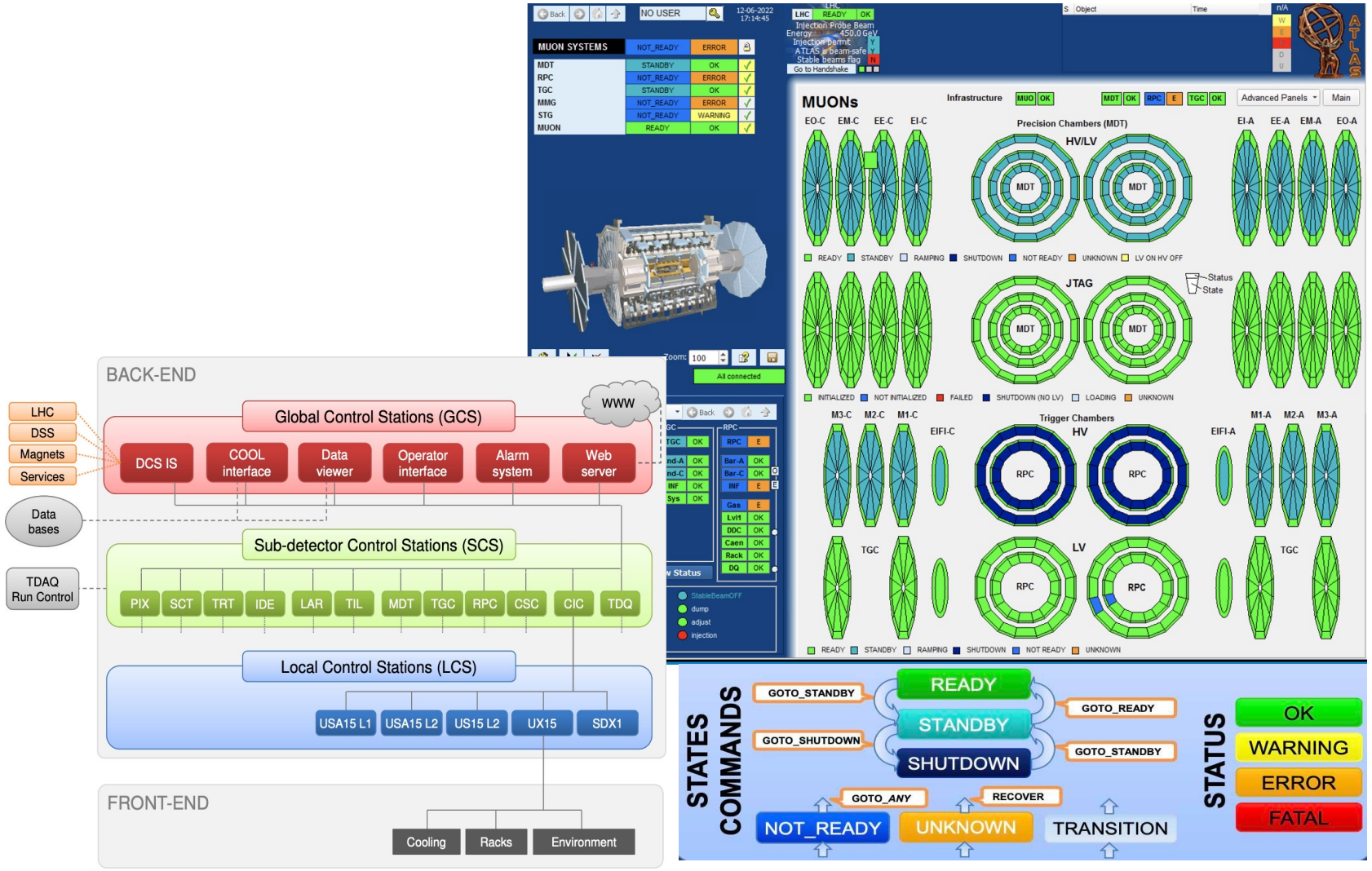
The HL-LHC requires major upgrades by the experiments to withstand the increased particle rate. The two major Atlas upgrade projects are the New Small Wheel and the BIS78A

Muon system upgrade goals:

- Improve the tracking efficiency in the high rate environment.
- Reduce fake triggers from background hits. Currently, intolerable end-cap muon trigger rate with 90% fake muon triggers.

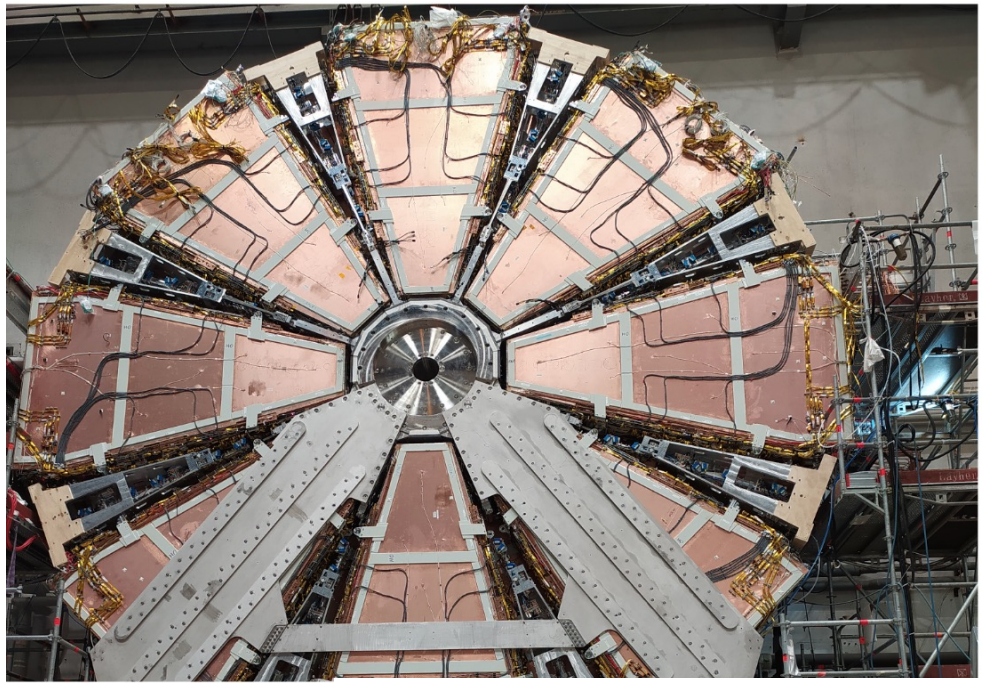
Detector Control System

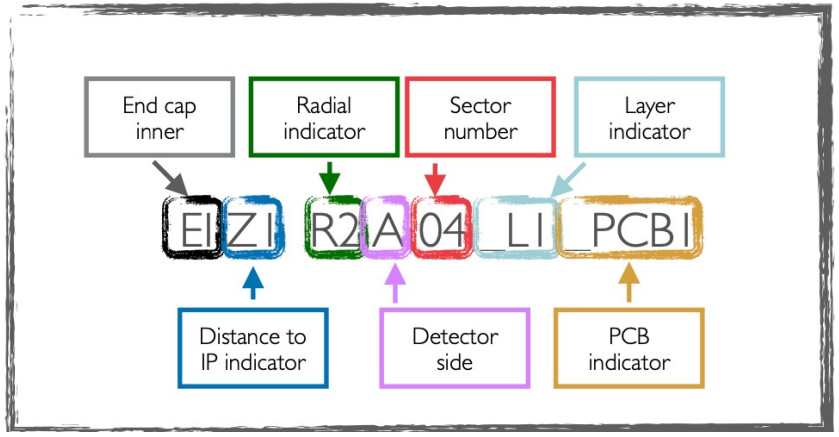
- Facilitate management of **implementation**, **operation** and **maintenance** by using standard building blocks
- Controls hierarchy:
  - 1. Front-End (FE): detector interface
  - 2. Local Back-End (BE): FE connection, readout, processing
  - 3. Sub-detector BE: grouping different technologies, standalone operation
  - 4. Global BE: interfaces to operators, storage and external facilities
  - **FSM(Finite State Machine)**

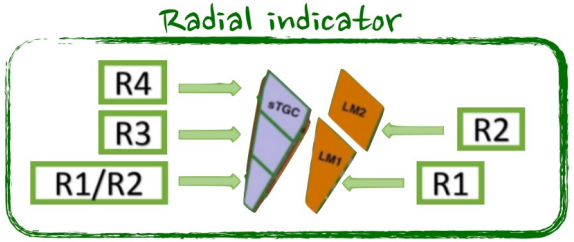


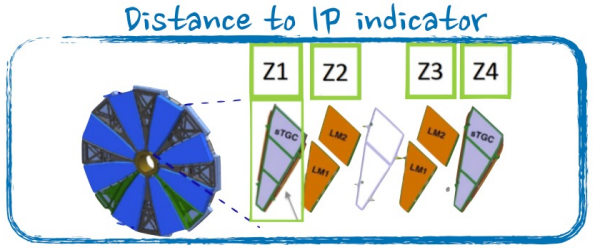
The New Small Wheel (NSW)

- the installation of NSW will reduce the trigger rate in the forward region (|η|>1.3) of the Spectrometer.
- Cope with future LHC Luminosities.
- Two new sub-detectors : MicroMegas(MM), small Thin Gas Chambers(sTGC).









MMG US15 Work

Mainframe's number of slots: 16
Can host 5 boards of A7038ST (3 slots) type or 16 of A7038A (1 slot) type.

- 4 A7038STP + 1 A7038STN Boards

4 x 32 = 128 channels for read-out
Mapping : 16 sectors x 1 quadruplet x 1 layer x 8 PCBs

1 x 32 = 32 channels for drift
Mapping : 16 sectors x 1 quadruplet x 2 radial segments

- 16 A7038AP Boards(NEW)

16 x 48 = 768 channels for read-out
Mapping : 16 sectors x 2 quadruplets x 3 layers x 8 PCBs

Mainframe	Boards
Mainframe 1 in Y.05-07.S2	16 × A7038AP
Mainframe 2 in Y.05-07.S2	4 × A7038STP 1 × A7038STN
Mainframe 3 in Y.05-07.S2	4 × A7038STP 1 × A7038STN

STG HV Scheme

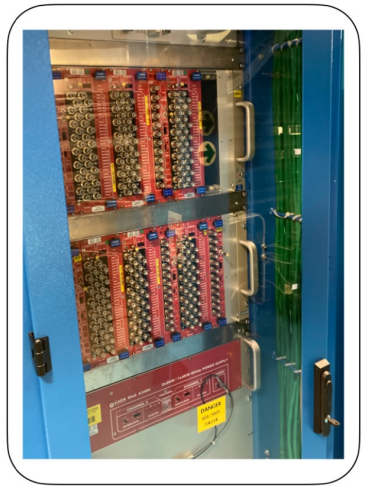
- The STG HV Scheme has been installed for both sides of NSW. For every side it consists of :

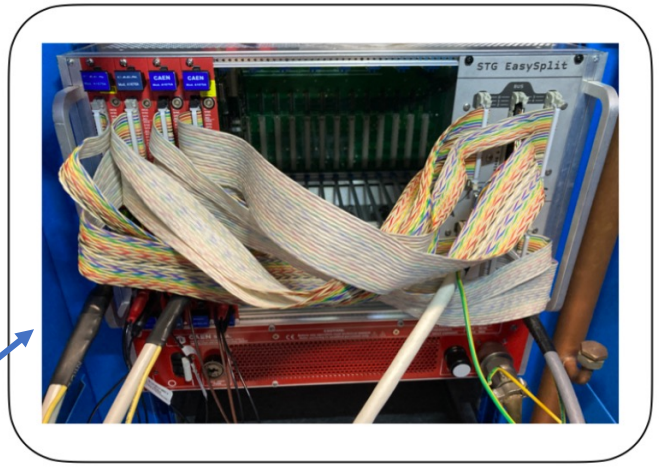
1. 1 S5427 Mainframe (USA15)
2. 2/side A1676 Branches (USA15)
3. 2 Crates per branch (UX15)

The crates are filled with two types of HV boards :

- A3535 (32 Channels)
- A3540 (12 Channels)
- 2 Generators(power and service)

- HV Splitter board due to communication issue with the CPU power of Branch Controller





x 2

S4527 Mainframe

A1676 Branch Controller

x 4

EASY 3000 crate

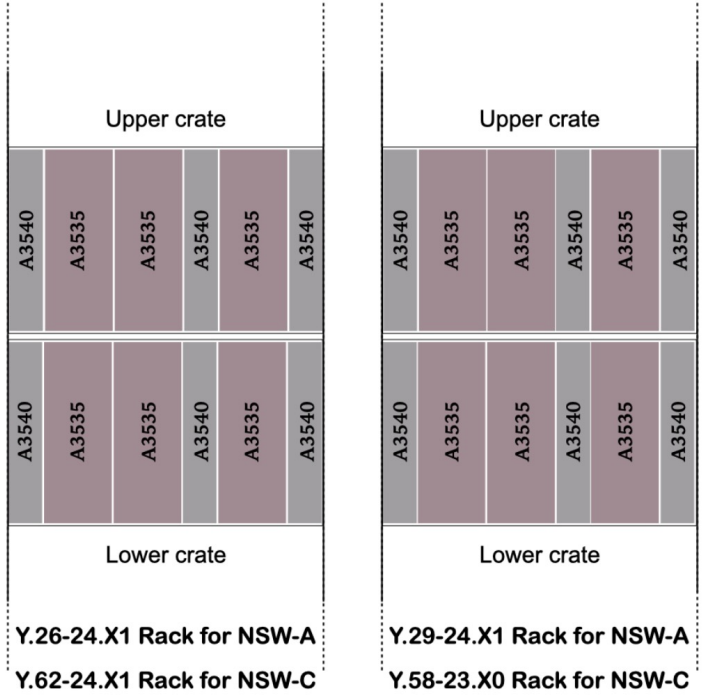
x 12

A3540 board

x 12

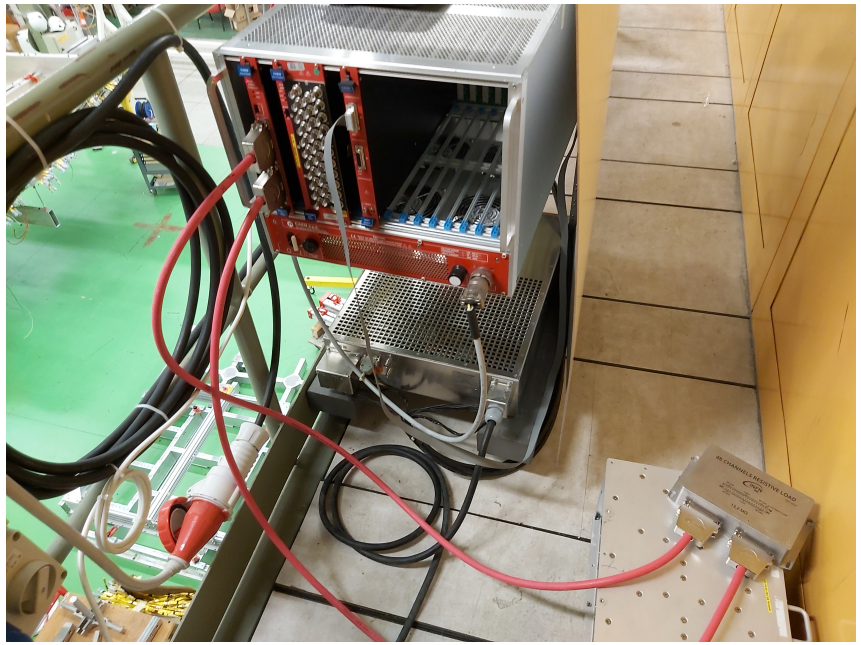
A3535 board

Arrangement of filled crates in the racks



MM HV Board Testing Site

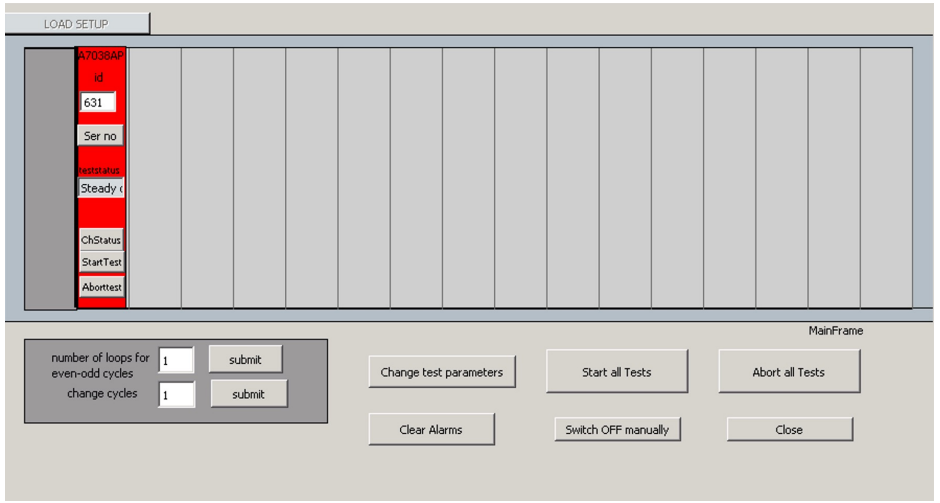
- Testing Site @ BB5:CERN
- One Mainframe with 16 slots
- 4 cables
- 2 loads (Resistors) , for the boards to start operating
- Testing 2 boards at the time

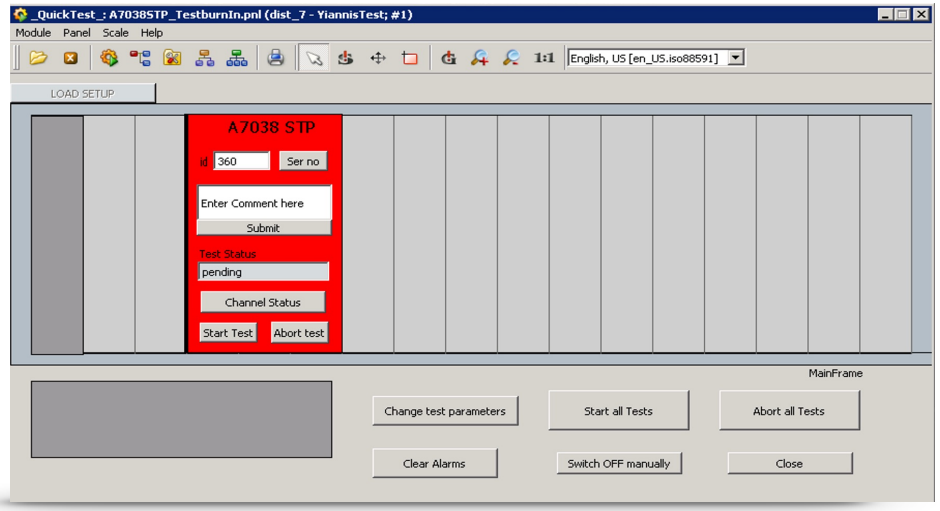


validation PC

NSW MM Board "Burn In" Validation Project

- Purpose : the boards can work under specific conditions with stable behavior.
- Development of a dedicated to the boards' validation project --Caen A7038(ST,A)-- at BB5.
- "One click" (start/stop) handling mechanism, to facilitate the validation process.
- "Settings Ease Configuration". Validation panel for the test of all the boards with the possibility to change the the test parameters whenever is needed.
- A root script has been developed in order to analyze the collected data **automatically** at the end of each run.





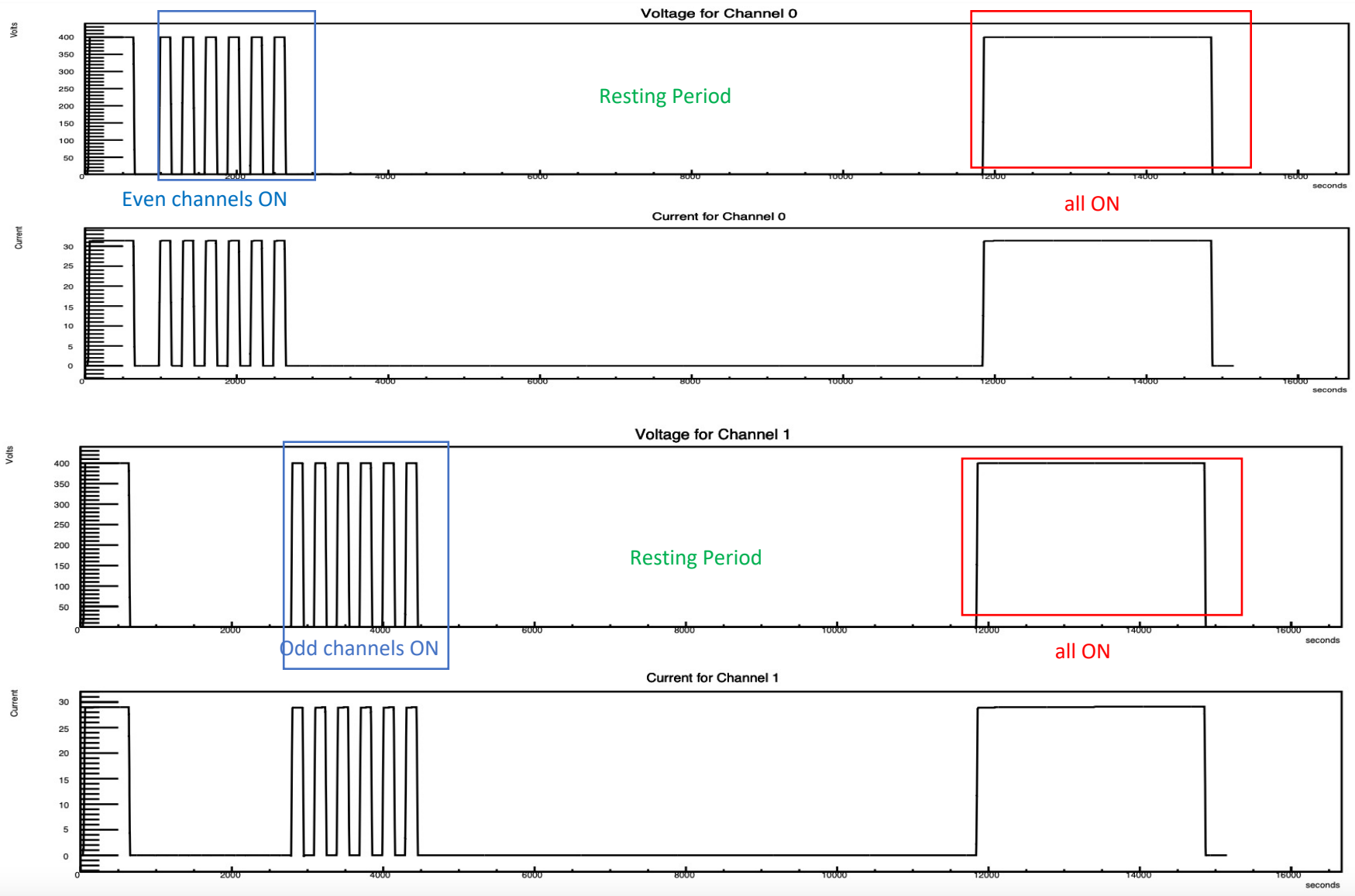
Test Steps

x3 steps 2-4 (before s5)

x3 steps 2-3 (before s4)

1. All channels of the board are ON for 10'
2. All ODD channels are OFF and EVEN are ON for 30'
3. All EVEN channels are OFF and ODD are ON for 30'
4. Switch OFF all channels for 2h.
5. Switch ON all channels for 50'
6. Switch OFF all channels

HV TESTING A7038AP BOARD(~4 HOURS)



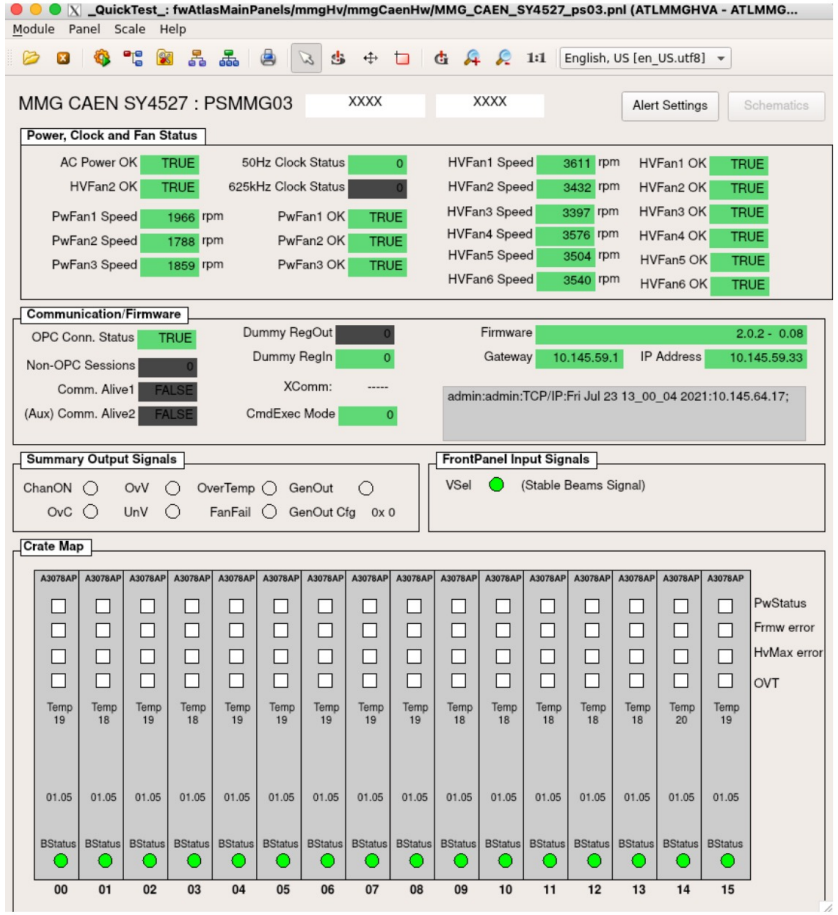
- 4 Batches(36 Boards)
- No issues
- Some more times on different durations for crosscheck

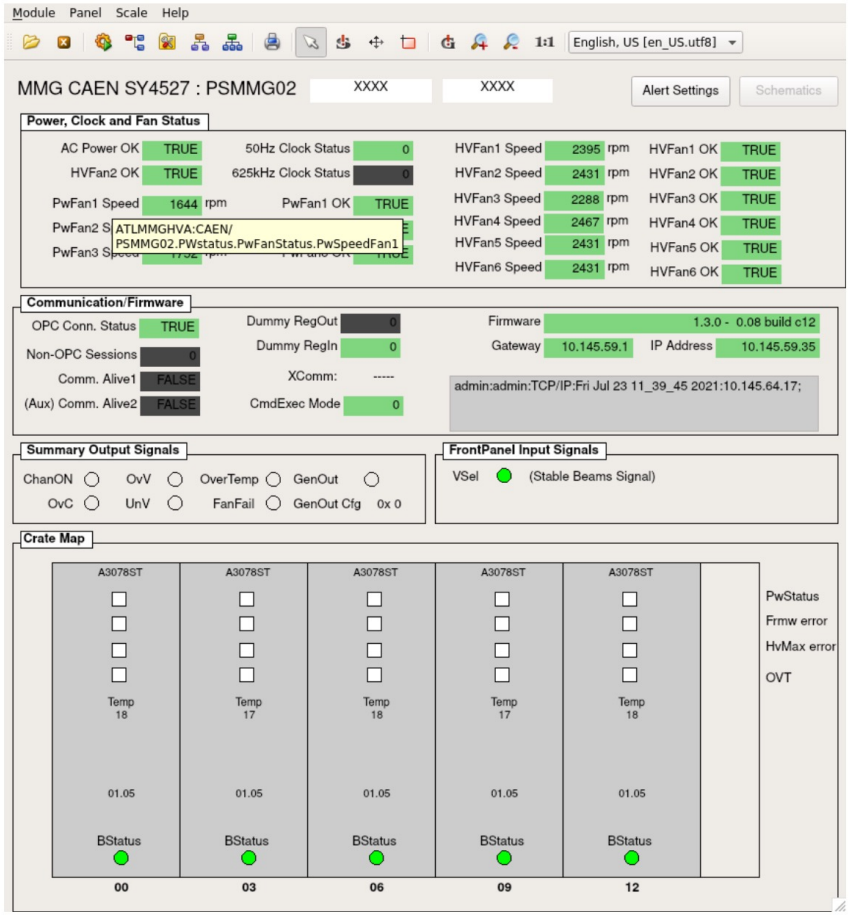
MMG CAEN EASY SYSTEM

- Low level structure :
  Data Points,archive,alarms for the new system.

- Create new panels for MMG Mainframes. Every panels includes the mainframe and boards parameters.

- The FSM consists of 3 nodes/one for every mainframe.



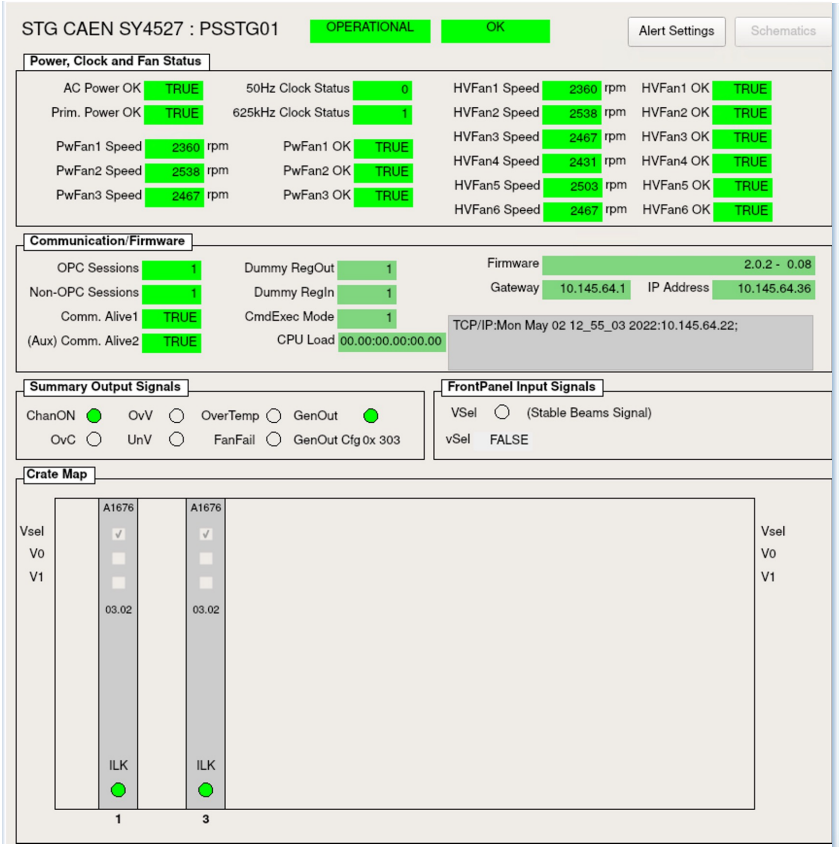


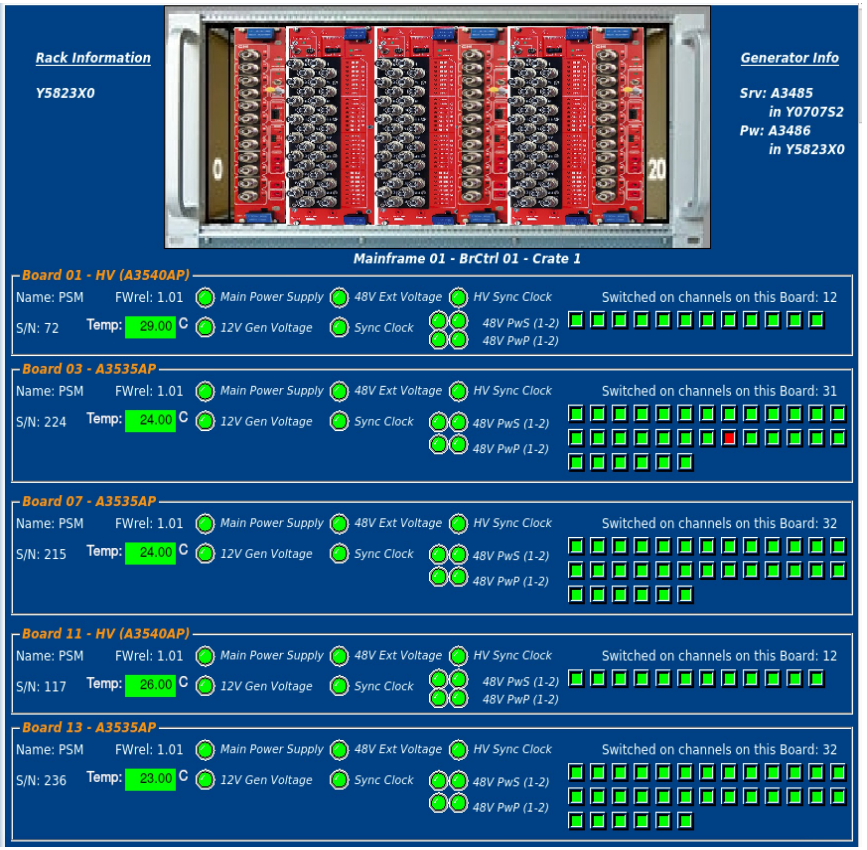
STG CAEN EASY SYSTEM

- Low level structure : Data Points,archive,alarms for the new system
- The FSM consists of 3 nodes :

1. 1 Mainframe
2. 2 branches
3. 2 crates per branch

- Panels have been modified accordinaly





STG CAEN 48V Generators

- Low level structure : Data Points,archive,alarms for the new Generators
  - Create new panels for the STG Caen Generators scheme
    - The FSM consists of four nodes
    - Two Generators/four channels per side
  - Generators can be operated directly from the FSM Commands

NSW CAEN Reset Network

- **CAEN Reset Network - What is the muon reset network ?**

The Reset Network allows to perform a simultaneous reset of boards/Branches/Mainframes per rack and sub-detector level.

- A system has been implemented following the Pre-Existing Muon logic.
- Two Reset Network Systems has been created for MMG and STG separate
- MMG Reset consists of the MMG HV Mainframes
- STG Reset consists of STG Branch Controllers and Mainframes for MMG LV and STG HV,LV

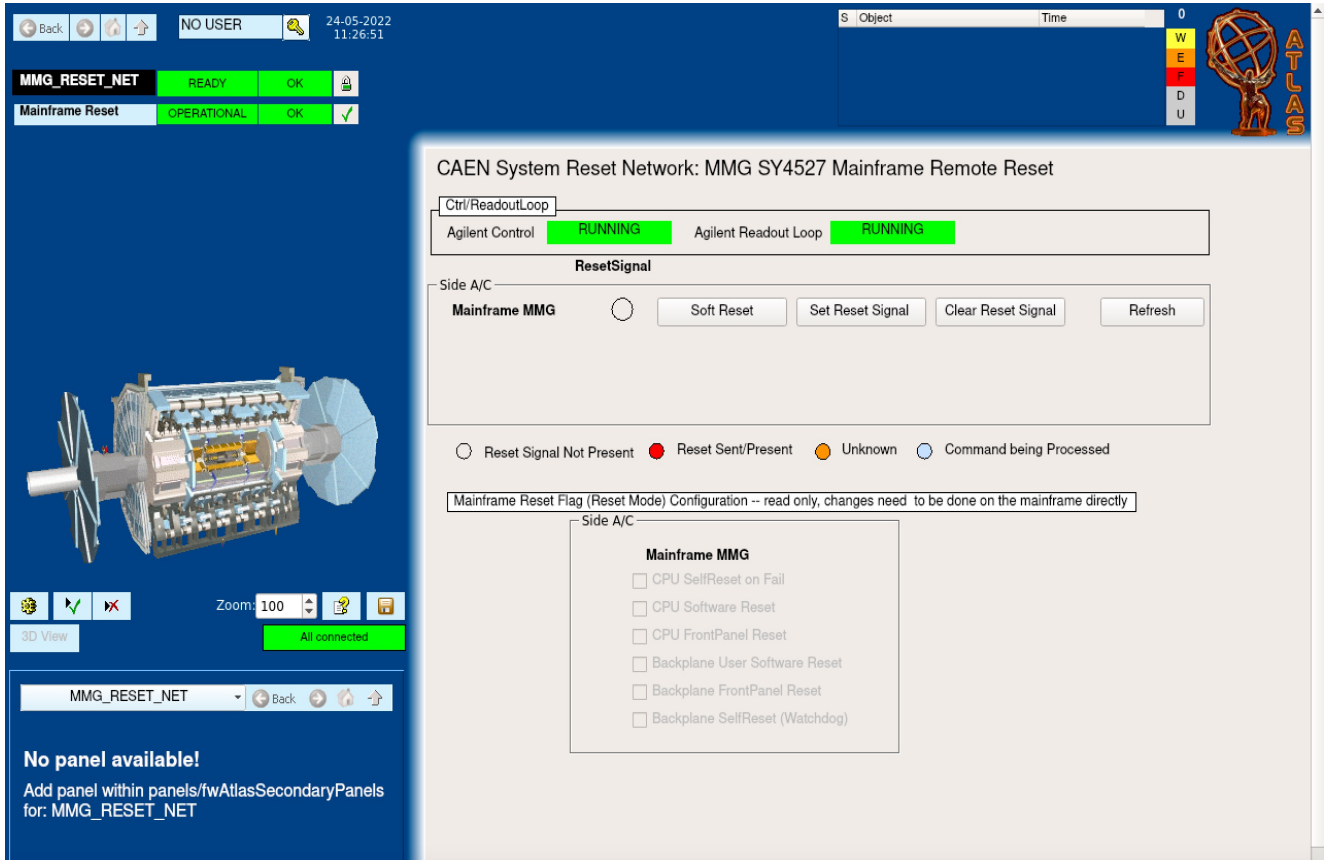
MMG CAEN Reset Network

The Mainframe(s) Reset

1 second to send the signal to the mainframe, while ~2 min to loop over all the chain including also the DCS.

SOFT Reset:
The signal is sent and then the flag is automatically reset! The specific reset touches the CPU without affecting the connected devices.

HARD Reset:
The signal is sent and the flag is not automatically reset! You have to **Clear** the reset after **1-2 seconds**. Everything connected to the mainframe will be switched OFF!



STG CAEN Reset Network

FSM consists of two nodes : one for Mainframe and one for the Branch Controllers

1. Mainframes Reset

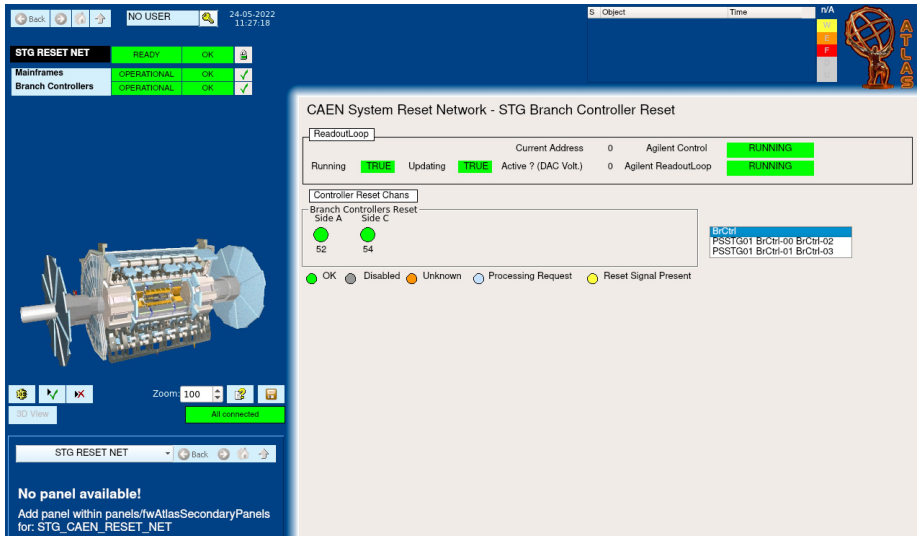
Same logic and procedure with the MMG.

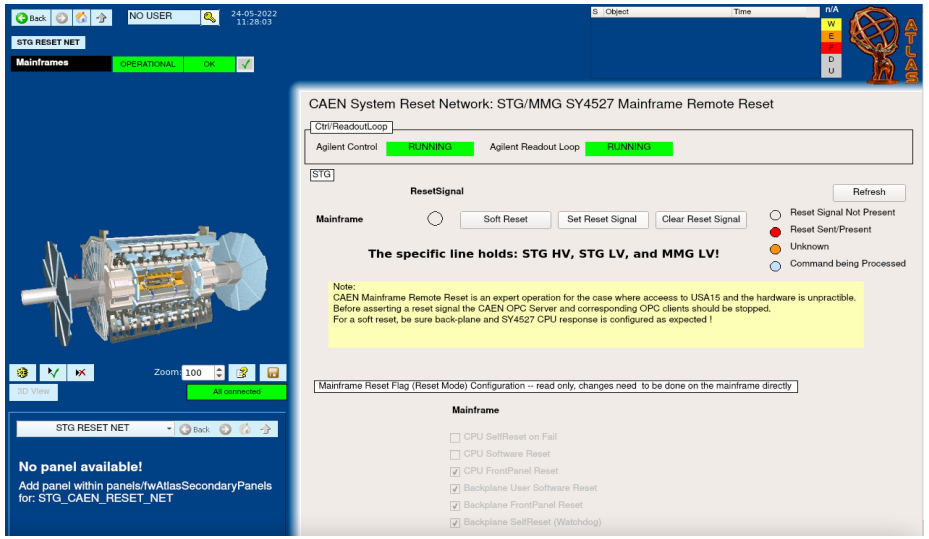
2. BRANCH CONTROLLERS Reset

Currently, two out of four lines are used! If the granularity increase also the other two will be used releasing Br02 and Br03 from their initial lines. Thus,

#52: Br00, and Br02 for side A

#54: Br01, and Br03 for side C





Summary

- All A7038AP Boards have been tested succesfully. No major issues have been found, and all the boards have been qualified and have been installed at P1.

  All the HV infrastructure is in place from September 2021, along with their dedicated DCS systems.
- The DCS System for both sides has fully integrated and is fully operational.
- NSW Reset Network has been installed and tested successfully and now is in use whenever is needed from the detector experts.
- The Caen Easy System is fully functional and operational for both sides of the NSW.

THANK YOU!!!

Backup