#### Segment Linking: A Highly Parallelizable Track Reconstruction Algorithm for HL-LHC

#### HEP 2022



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#### Intro to HL-LHC Challenges

- High Luminosity LHC (HL-LHC): Planned LHC upgrade with up to ×8 current luminosity.
- Higher luminosity  $\Rightarrow$

More simultaneous interactions (PU):  $\langle PU \rangle_{LHC} \leq 70 \rightarrow \langle PU \rangle_{HL-LHC} \approx 200$ 

More PU ⇒

#### Increased computational complexity $\Rightarrow$

- Increased timing.
- Increased cost.





#### Heterogeneous Computing

- Run 2 computational resources dominated by CPU ⇒
  Exploit alternative processing units: FPGA, GPU, etc.
- Application of GPU computing in CMS:
  - Pixel track & vertex reconstruction (patatrack).
  - Outer tracker strip local reconstruction.
  - Electromagnetic calorimeter (ECAL) reconstruction.
  - Hadronic calorimeter (HCAL) reconstruction.
- Significant reductions in timing (~25%) for Run 3 CMS High Level Trigger (HLT)<sup>[\*]</sup>.

[\*]: <u>CMS-TDR-022</u>

anl

 $e_{0}$ 

Alternative processing units: Cheaper per nominal compute operation ⇒
 Significant cost reduction (~35–75%)

projected for HL-LHC computational resources[\*].



## Segment Linking Overview

- Leverage GPU performance in track reconstruction →
  Algorithm architecture suitable for parallelization.
- Segment Linking:

Sanl

A highly parallelizable track reconstruction algorithm

- Moves away from sequential Kalman filter based algorithms → <u>mkFit project</u> tries to make the most out of that.
- Relies on local hits in the tracker to build short tracks.
- Short tracks linked to form progressively longer tracks.
- Selects objects from intermediate collections to create a Track Candidate collection with high efficiency and low fake rate.
- Inspired by <u>XFT algorithm</u> in the CDF at the Tevatron.
- Prototype presented in <u>ICHEP 2016</u>.

#### **CMS Outer Tracker @ HL-LHC**

0.0

E<sup>1200</sup>

800-

600

400-

200

- CMS HL-LHC
  outer tracker
  ideal for algorithm
  application:
  - Closely-spaced
    sensors ⇒
    - Local hits (stubs) above p⊤ threshold (0.8 GeV).
- Stubs instead of hits ⇒
  - Up to ×7.5 reduction of combinatorics:
  - E.g. 5.9k vs. 36k in 1st layer.



### Linking Stubs



17 Jun 2022

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## Linking Segments



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## Linking Pixel Segments



#### Track Candidate Collection

- Final Track Candidate (TC) collection includes:
  - Pixel Quintuplets (pT5) → Performance driver.
  - Unlinked **Pixel Segments (pLS)**  $\rightarrow$  Important at low p<sub>T</sub> and high |η|.
  - Pixel triplets (pT3)
    → Regain low p<sub>T</sub> efficiency.
  - Quintuplets (T5)
    - → Important for **displaced** tracks.



**Outer tracker** 

Outer tracker

**Inner tracke** 

**Inner tracker** 

**Inner tracker** 

#### **Physics Performance: Efficiency**

- Efficiency vs.  $p_T \& \eta$  checked in  $t\bar{t}$  sample in PU200.
- Denominator: All simulated tracks passing:
  - $|d_z| < 30 \text{ cm}$
  - $|d_{xv}| < 2.5 \text{ cm}$
- Numerator: Simulated tracks matched to TC track (>75% hits).



#### **Physics Performance: Efficiency**

- Efficiency vs. d<sub>xy</sub> checked in muon gun sample with displaced vertex uniformly distributed in a (5 cm)<sup>3</sup> cube around the interaction point.
- Denominator: All simulated tracks passing:
  - $|d_z| < 30 \text{ cm}$
- Numerator: Simulated tracks matched to TC track (>75% hits).



#### **Physics Performance: Fake Rate**

- Fake rate vs.  $p_T \& \eta$  checked in  $t\bar{t}$  sample in PU200.
- Denominator: All TC tracks.
- Numerator: TC tracks NOT matched to simulated track (>75% hits).



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#### **GPU Architecture**

D	CPU	GPU
	$\mathcal{O}(64)$ cores	O(100) - O(1000) cores
	~2 Flops (Intel Xeon)	15 Flops (NVIDIA Tesla V100)
	Low latency	High latency (device-host memory transfers)
	Good for serial processing	Good for parallel processing

- $\Rightarrow$  GPU programming requires:
  - Suitable algorithm (=parallelizable).
  - Programming tricks
    (≈clever memory usage).
- Efficiently take advantage of:
  - Multitude of computing units.
  - Different memory levels (size vs. speed trade-off).



## **GPU Implementation**

- Data stored in Structure of Arrays (**SoA**) format  $\Rightarrow$ Appropriate for parallelized access.
- Custom cache allocation for optimized memory assignment.
- Truncate number of objects based on final occupancy ⇒
  Minimize memory footprint.
- Full implementation on NVIDIA Tesla V100: <u>https://github.com/SegmentLinking/TrackLooper</u>



## **GPU Implementation**

• Kernels: Independent set operations on separate processing element.



- Each kernel = Single Instruction, Multiple Data (SIMD) →
  Same steps applied to different objects →
  Local nature of Segment Linking.
- Speed up by **multi-streaming**: Run parts of kernels in different streams.
  - Memory transfers also "hidden" by concurrent computations.



# Timing

- Timing measurements in  $t\bar{t}$  sample in PU200.
  - Only algorithm execution →
    Final device to host memory transfer excluded.
- 1-stream: t ≈ 32 ms
- 8-stream: t ≈ 26 ms
  - ~20% timing improvement by exploiting multi-streaming.
- Comparable with latest CMS tracking (~40 ms) on CPU.
- Comparable also price-wise →
  2× 32-core Skylake Gold Xeon processors ≈ NVIDIA Tesla V100.

#### Future Updates

- Physics-wise:
  - Stretch performance to its limits  $\rightarrow$  Further selection optimization for **better efficiency** and **lower fake rate**.
  - Improved **displaced tracks** reconstruction.
  - Incorporate latest developments (e.g. patatrack pixel tracks)
- Computing-wise:
  - Optimize algorithms for complex physics parameter calculations.
  - Extend usage of alternate data types → Half precision.
  - Improve **memory coalescence** ⇒ Timing reduction.
- The Great Design:
  CMS software integration for HLT and offline usage.

## Summary

- Segment Linking:
  - A highly parallelizable track reconstruction algorithm.
  - Aimed at facing HL-LHC challenges.
  - Successfully implemented on GPU.
  - Competitive physics performance (efficiency and fake rate).
  - Timing comparable with current CMS HLT tracking algorithms.
  - More improvements and CMS integration planned for the future.